CLAIMS

What is claimed is:

1. A method for controlling an associated circuit, comprising:

providing a clock waveform to the associated circuit that transitions between normally high and low levels over a cycle in a first operating mode; and

modifying the clock waveform provided to the associated circuit to include an intermediate level between the normally high and low levels over a cycle in a second operating mode.

2. The method of claim 1, further comprising implementing a delay that controls the duration for which the clock waveform is provided at the intermediate level in the second operating mode.

3. The method of claim 1, further comprising:

receiving a mode selection signal; and

controlling the operating mode based on the mode selection signal.

4. The method of claim 3, the mode selection signal corresponding to an enable signal associated with a burn-in process.

5. The method of claim 1, further comprising controlling the clock waveform to be provided an intermediate level that mitigates process variations in the associated circuit.

6. The method of claim 1, a duration of the cycle in the second operating mode having a greater duration than the cycle in the first operating mode.

7. The method of claim 6, the duration of the cycle in the second operating mode being at least ten times greater in duration than the cycle in the first operating mode.

8. The method of claim 1, the second operating mode corresponding to a burn-in process.

9. The method of claim 1, the intermediate level of the clock waveform being provided to the associated circuit by a voltage source.

10. The method of claim 1, the clock waveform being provided to a plurality of associated circuits, each of the associated circuits having a respective precharge device, the method further comprising controlling the precharge devices in the plurality of associated circuits based on the clock waveform provided according to a selected one of the first and second operating modes.

11. The method of claim 1, further comprising:

causing a precharge device of the associated circuit to partially conduct based on the intermediate level of the clock waveform provided in the second operating mode, such that the precharge device operates as supplemental keeper to mitigate at least one of noise and leakage in the associated circuit during the second operating mode.

12. A clock generator comprising:

a driver that provides an output waveform to drive at least one associated circuit based on at least one control signal; and

a control network that provides the at least one control signal to cause the driver to provide the output waveform to transition between normally high and low levels during a first operating mode, the control network provides the at least one control signal to cause the driver to provide the output waveform to include a temporary intermediate level that is between the normally high and low levels during a second operating mode.

13. The clock generator of claim 12, further comprising a delay element that controls a duration for which the output waveform is at the intermediate level during the second operating mode.

14. The clock generator of claim 12, further comprising an associated circuit that includes a precharge device that charges an associated node based on the output waveform provided by the driver, the precharge device partially conducts according to the intermediate level during the second operating mode, thereby operating as a

supplemental keeper to mitigate noise in the associated circuit during the second operating mode.

15. The clock generator of claim 12, further comprising a voltage source that provides the output waveform at the intermediate level during the second operating mode.

16. An integrated circuit comprising the clock generator and the associated circuit of claim 12.

17. The integrated circuit of claim 16, the associated circuit further comprising a precharge device that provides a charge to an associated node of the at least one associated circuit based on the output waveform, whereby noise in the associated circuit is mitigated during the second operating mode.

18. The integrated circuit of claim 17, the associated circuit comprising a domino logic circuit that includes the precharge device, the second operating mode corresponds to a burn-in process, such that the output waveform at the intermediate level mitigates noise to facilitate evaluation of the domino logic circuit during the burn-in process.

19. The integrated circuit of claim 17, the associated circuit further comprising a plurality of associated circuits, each of the plurality of associated circuits including a respective precharge device that operates as a supplemental keeper during the second operating mode to mitigate noise in the respective associated circuit.

20. A system for providing an output waveform, comprising:

means for providing a first waveform at an output that transitions between normally high and low levels during a first operating mode;

means for providing a second waveform at the output to include an intermediate level between the normally high and low levels during a second operating mode; and

means for selecting between the first and second waveforms based on a mode selection signal.

21. The system of claim 20, further comprising means for charging an associated node based on the waveform at the output, the means for charging partially conducts based on the intermediate level of the second waveform during the second operating mode, thereby operating as a supplemental keeper to mitigate noise in circuitry associated with the means for charging.

22. The system of claim 20, further comprising means for controlling the second waveform to be provided at an intermediate voltage level between the normally high and low levels to mitigate process variations in at least part of the system.

23. The system of claim 20, further comprising means for controlling a duration for which the control signal is provided at the intermediate level.

24. An integrated circuit comprising the system of claim 20.